

**HOLD FOR RELEASE UNTIL SEPTEMBER 12, 2006**
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**NEC Electronics Introduces Industry's First  
 Ultra-Low-Power 55-nanometer Embedded DRAM Technology**

***Optimized for Low Power and High Performance, Embedded DRAM Solution  
 Targets Next-Generation Mobile and Digital Consumer Devices***

**KAWASAKI, Japan, SANTA CLARA, Calif., DÜSSELDORF, Germany, September 12, 2006** —

NEC Electronics Corporation and its subsidiaries in North America and Europe, NEC Electronics America, Inc. and NEC Electronics (Europe) GmbH, today announced the industry's first 55-nanometer (nm) CMOS-compatible embedded DRAM (eDRAM) technology, UX7LSeD. An enhancement to NEC Electronics' patented metal-insulator-metal (MIM2) technology, the new eDRAM process is the industry's first combination of hafnium silicate film and nickel silicide, which has resulted in reduced power consumption and leakage current at this advanced node. Optimized for high-speed, low-power operation, the new process can be applied to system-on-chip (SOC) devices designed for a broad range of products—from mobile equipment such as cell phones and mobile handheld devices to digital consumer devices such as gaming consoles.

“By delivering the only CMOS-compatible eDRAM at the 55 nm node, NEC Electronics is enabling designers to overcome the limitations of embedded SRAM and discrete DRAM components to achieve high-performance SOCs for next-generation applications,” said Takaaki Kuwata, general manager, Advanced Device Development Division, NEC Electronics. “A combination of innovative materials and our mature MIM2 process, the new eDRAM offers low leakage power in a high-speed, high-density solution. In fact, NEC Electronics already has earned four patents for the MIM capacitor, the silicided eDRAM cell, the bit-contact structure and the MIM lower electrode structure.”

**Technology Advances Reduce Power Consumption, Design Risks**

The introduction of hafnium silicate film to the embedded DRAM process has allowed NEC Electronics to reduce leakage current while increasing on-current by as much as 20 percent.

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Reducing the leakage current is an important factor to maintaining reasonable data retention time in eDRAM macros. The new manufacturing material also has allowed NEC Electronics to continue to use polysilicon gates, as opposed to metal gates, which helps to reduce process risks for volume production.

The use of nickel silicide, a material suitable for aggressively scaled structures, helps to maintain low parasitic resistance of the scaled-down eDRAM cell and peripheral circuits and also reduce standby and operating power. Furthermore, the high dielectric constant (high-k) technology applied to the eDRAM cell transistor boosts its performance, reduces leakages and suppresses variability, as the work-function modulation effect of high-k is fully exploited to reduce transistor channel concentration.

These new materials and the proprietary MIM2 technology are enabling NEC Electronics to deliver robust eDRAM solutions with smaller cell sizes, higher memory integration, ample storage capacitance and lower cell heights, and all the while maintain the merits of existing eDRAM technology, such as CMOS compatibility, low power and high-speed random access.

### **NEC Electronics' Unique eDRAM Technology Benefits**

NEC Electronics' eDRAM uniquely combines DRAM density with SRAM-like performance, low latency and robust performance. With lower power consumption and a lower soft error rate than embedded SRAM, NEC Electronics' eDRAM has blocks that can be rotated in any orientation on a chip to simplify integration with other on-chip components while preserving the performance and power consumption benefits afforded by NEC Electronics' process. The upper metal layers of an ASIC also can be routed over the top of eDRAM blocks to simplify chip design, improve timing and conserve silicon.

The NEC Electronics process employs both a cylindrical-type stacked capacitor structure that ensures high yields and a low-temperature MIM2 capacitor that accelerates performance. The MIM2 technology uses zirconium oxide (ZrO<sub>2</sub>), a dielectric material with a high-k factor that allows the embedded DRAM's smaller bit cells to retain storage capacitance. Unlike its commodity DRAM process, NEC Electronics' eDRAM process uses the same structure as its standard CMOS process, and thus is fully compatible with it. This compatibility dramatically reduces turnaround time by minimizing the number of process steps needed to add eDRAM.

### **Availability**

NEC Electronics' 55 nm 8-megabit (Mb) and larger embedded DRAM macros are expected to be available for volume production in the second half of 2007. More information can be found at [www.am.necel.com/edram](http://www.am.necel.com/edram). (Availability is subject to change.)

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### **About NEC Electronics**

NEC Electronics Corporation (TSE: 6723) specializes in semiconductor products encompassing advanced technology solutions for the high-end computing and broadband networking markets, system solutions for the mobile handset, PC peripheral, automotive and digital consumer markets, and multi-market solutions for a wide range of customer applications. NEC Electronics Corporation has 25 subsidiaries worldwide including NEC Electronics America, Inc. ([www.am.necel.com](http://www.am.necel.com)) and NEC Electronics (Europe) GmbH ([www.eu.necel.com](http://www.eu.necel.com)). For additional information about NEC Electronics worldwide, visit [www.necel.com](http://www.necel.com).

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