

Description

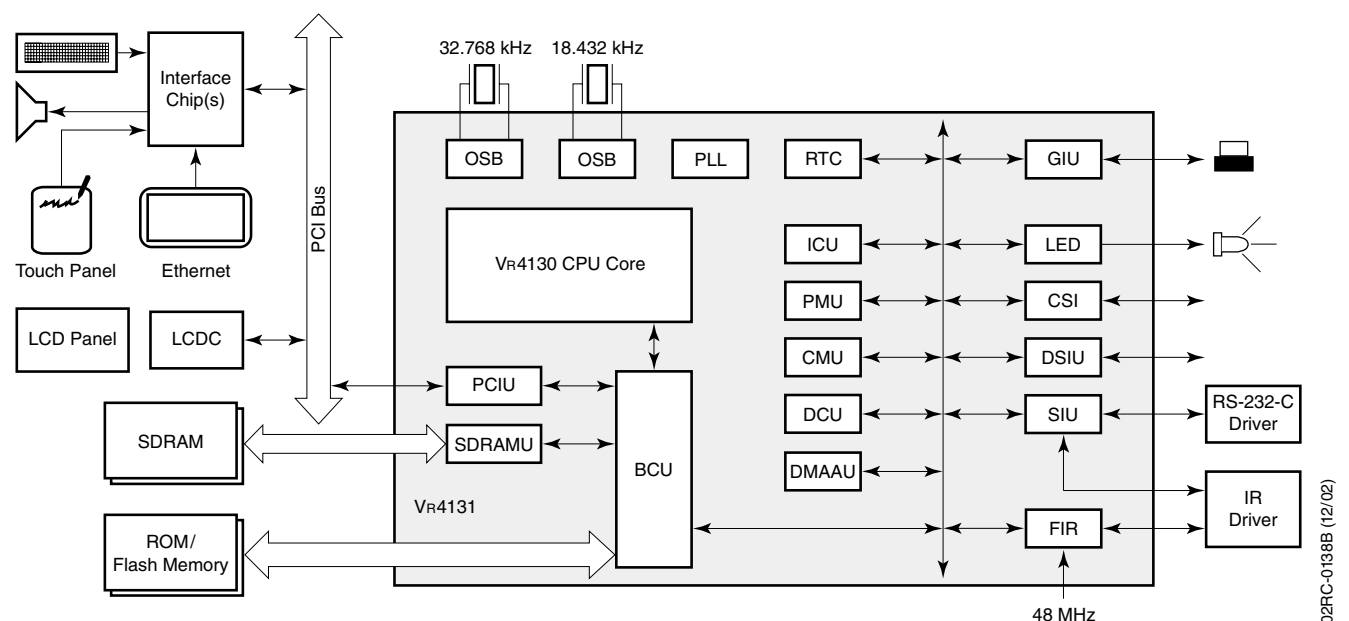
The VR4131 is the MIPS per mW leader of NEC Electronics America's VR Series™ product line. This high-performance 64-bit RISC microprocessor employing the MIPS I, II, III, and MIPS16 instruction sets delivers 1545 MIPS per watt, one of the highest-performance, lowest power ratios currently available. In addition to an ultra-low-power-consuming VR4130 CPU core, the device has cache memory, two-way superscalar pipeline, memory management unit, and peripherals including a DMA interface, serial interface, IrDA® interface, and real-time clock, among others. The VR4131 also has a 32-bit external memory bus and supports a PCI bus interface for external devices, allowing easy embedded systems development.

Specifications

- High performance/low power ratio of 1545 MIPS per watt
- Maximum power consumption
 - 220 mW at 200 MHz (typical)
- High-performance operation
 - 340 Dhrystone MIPS at 200 MHz
- Storage systems
- Wireless LAN access points
- Network interface cards (NICs)
- Server farms
- Information appliances
 - Portable Internet appliances
 - Pocket PCs
- Control applications
- Supply voltage: 1.5 V (internal) and 3.3 V (external)
- 224-pin FPBGA (16 mm x 16 mm)
- Pin-compatible with NEC's VR4122 (except N-wire)
- Full industrial -40°C to +85°C ambient operating temperature range

Applications

Block Diagram



Features

CPU

- 64-bit MIPS RISC CPU core (VR4130 equivalent)
- Two-way superscalar pipeline
- Internal 64-bit data processing
- Big and little endian modes

Powerful MIPS Instructions

- MIPS I, II, III instruction sets (without FPU instructions)
- MIPS16 instruction set
- High-speed product/sum instructions
- Multiply-add instruction for product-sum operation of $32 \times 32 + 64$ bits with one clock

Clocks

- External clock input: 32.768 kHz
- Internal CPU core and peripheral unit operation: 18.432 MHz
- IrDA interface: 48 MHz
- Programmable clock management for each on-chip peripheral

Power Management Modes

- Full speed: normal operation with all clocks functional
- Standby: internal clocks stop except for timer or interrupt-related clocks
- Suspend: bus clock and internal clocks stop except for timer or interrupt-related clocks
- eXsuspend: same as Suspend mode, except that can turn off the internal PLL
- Hibernate: clocks generated by the CPU core stop function

Memory

- On-chip two-way set associative cache: 16 KB instruction and 16 KB data
- Synchronous DRAM interface with access at 100 MHz
- Memory controller for ROM, synchronous DRAM, and flash memory
- Independent ROM and RAM with 16-/32-bit bus width
- Cache locking for critical code execution

Peripherals

- 32-bit PCI version 2.1 interface operating at 33 MHz
- Fast IR processing in compliance with IrDA specification 1.1
- DMA controller
- Interrupt controller
- General-purpose I/O ports
- Two-channel 16550-compatible serial interface
- Serial interface
- Serial debugging interfaces
- Synchronous three-line serial clock
- Real-time clock

Ordering Information

Part Number	Package
μPD30131F1	224-pin FPGA

Development Systems

RockHopper™ family development systems are available for purchase. Includes two options with or without Baseboard. See the RockHopper family product brief (Document No.: 50398-2) for more details.

Part Number	
DDB-VR4131A	Complete kit with baseboard
CMB-VR4131A	Kit without baseboard

VR4131

64-Bit MIPS® RISC Microprocessor

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