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**ISSP - a new ASIC technology
for mid-volume quantities**

ISSP - ASIC technology for mid-volume designs

Christoph Hecker of NEC Electronics describes how the Instant Silicon Solution Platform provides an alternative to ASICs and FPGAs combining high system frequencies and reduced costs.

Up to now, there have been three main approaches to developing custom circuits: standard-cell ICs, field programmable gate arrays (FPGAs) and gate arrays. Each of the three technologies will have advantages and disadvantages for a particular application and these need to be weighed up carefully for each individual development project.

Standard-cell ICs allow you, for instance to achieve highest performance for optimal area efficiency. This result can be obtained only through the investment of substantial development resources. In a standard-cell IC design, it is not enough to ensure functionality alone; the demands on process technology are also increasing all the time.

In the deep sub-micron (DSM) performance class (<0.25µm design rule length), the designer is confronted with effects that can only be handled with huge additional effort. These DSM effects (eg, migration, antenna effects) are evoked by the physics of the ever-smaller structures. That is why they are taken care of at the back-end of a design process with special development tools.

Optimal design

As handling these tools requires detailed know-how, NEC will perform this task for customers. Even with this assistance, it is obvious that the greater the developer's own know-how in this area, the more likely he will be obtain an optimal design (with respect to minimized area and optimized performance). Because of the effort involved, the design turnaround time (TAT) becomes one of the decisive factors in a project plan.

Another aspect that must be taken into

account is the one-time or non-recurring engineering (NRE) cost associated with standard-cell ICs. This cost, mainly for making the photolithography masks, can easily reach several hundred thousand euros for masks with design rule lengths of 0.18µm or less. It can only be recouped by selling a correspondingly large number of chips.

FPGAs enter the fray

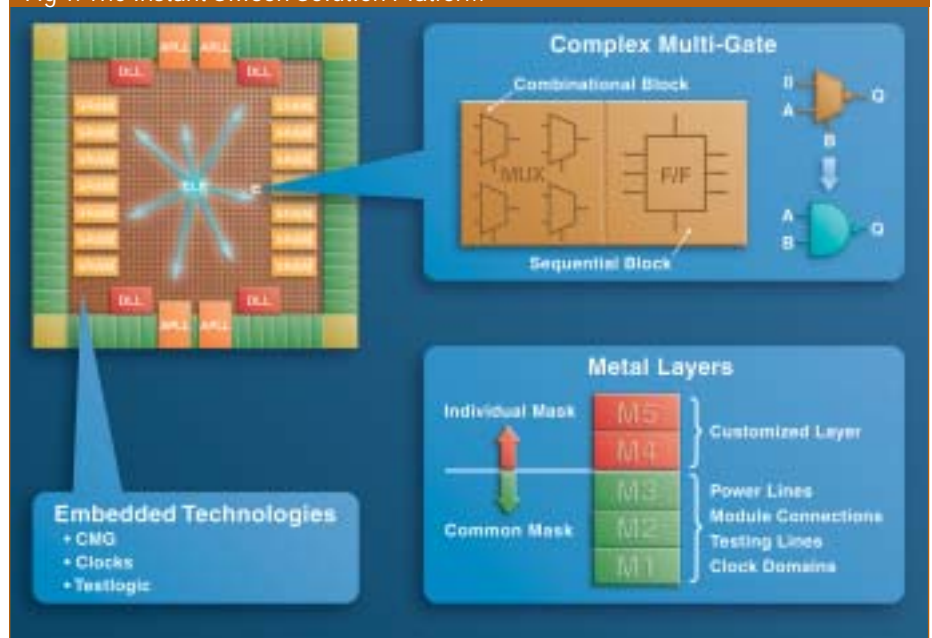
This is where FPGA manufacturers enter the fray, offering solutions that at first glance appear far less expensive. In contrast to standard-cell ICs and gate arrays, FPGAs have the advantage of being programmable, so that mask costs fall away. This is a benefit during the development or system test phases, because a design can still be modified at this stage without sig-

nificant extra cost. But for FPGAs too, integrating very complex designs requires a very big effort.

In addition, the high system frequencies typically achieved with standard-cell ICs can seldom be attained with FPGAs. The much-vaunted cost benefit of FPGAs disappears when volume production starts, if not earlier. That is when the aspects of FPGAs that initially seemed so attractive turn out to have serious downsides. The programmability means a larger area of silicon, higher power consumption and a larger and more expensive package to accommodate the greater number of pins required. Even for relatively small volumes, mask-programmable ASIC solutions prove to be the cheaper variant for volume production.

In contrast to standard-cell ICs, gate-

Fig 1: The Instant Silicon Solution Platform



array technologies give designers a wafer with ready-made gate structures, eg, in a 'sea-of-gates' architecture, that are complete but for the metallization layer. All that is left to do is to implement the custom circuit by wiring the gates on the metallization layer. Compared with standard-cell ICs, this technology has the disadvantage of lower area efficiency and lower performance.

On the other hand, the development costs of a gate array are far less than for a standard-cell IC, since the circuit implementation only requires the addition of metallization layers, and thus a significantly reduced number of design steps.

The development effort for gate array is also very low because it can be largely automated. NEC, for instance, offers gate array technologies, down to 0.25 μ m design rule lengths based on a 'sea-of-gates' architecture, with clear cost benefits over FPGAs as soon as the product goes into volume production. These technologies are also specifically targeted at transferring FPGA designs to gate-array technologies. The system frequencies achieved with gate arrays are more than likely to exceed those of current FPGA technologies.

Nonetheless, until recently, there was no really cost-effective alternative to standard-cell ICs if customers wanted ASICs with high system frequencies (from about 150MHz) and wanted to have them quickly.

ISSP raises performance

ISSP, NEC's Instant Silicon Solution Platform has been created to close this gap. ISSP offers higher system performance - up to 300MHz system frequency - in a 0.13 μ m technology. The NRE costs are only about a tenth of those for a similar design using a standard-cell IC. At the same time, unit costs are many times lower than for a comparable FPGA.

The typical, process-related hurdles of a 0.13 μ m ASIC design are avoided by taking a new approach, so that the designer only has to worry about the implementation of the actual circuit. Moreover, an ISSP design can be moved into volume production extremely quickly. It has a design turnaround time of roughly a week for first samples and another month for volume production.

ISSP is based on the same process that is used for NEC's CB-12 standard-cell ASIC technology. It offers a technology with a design rule length of 0.13 μ m (drawn) that can be as cost-effective for small batches as for volume production. The ISSP product series currently includes three different

Fig 2: ISSP master line-up

Master	Usable Logic	16 Kbit SRAM	Total CMG	APLL(#)		DLL(#)
				High Speed	Middle Speed	
μ PD65701	215 K	16	33.172	3	1	8
μ PD65702	510 K	48	71.927	3	1	8
μ PD65703	1,084 K	64	168.068	3	1	16

sized masters with different integration densities - see figure 2.

For the ISSP approach, NEC developed complex multi gates (CMGs) consisting of a combinatorial and a sequential section. Using CMGs, the actual circuit can be implemented at a higher abstraction level, free from the constraints DSM effects. With the complex gate structure predefined in this way, DSM effects no longer have an impact on the implementation of the design. NEC is a leading developer and manufacturer of standard-cell ASICs and has applied its massive know-how and experience in this field to implementing CMGs in ISSP.

In addition to CMGs, ISSP also contain preintegrated, customer configurable SRAMs of up to 1Mbit on one ISSP master. Each of the masters is equipped with 4 analog phase-locked loops (PLL) with up to 400MHz output frequency and up to 16 digital-locked loops (DLL) that can be used as a slave for a DDR interface.

Easing DFT and DSM

Today's FPGA technologies are not really a proposition at system level with speeds above 100MHz. That is why customers requiring this performance class have had no choice but to use standard-cell ASIC technologies. When standard-cell ASIC development techniques are used, a first functional verification is usually carried out using very expensive FPGA-based hardware emulators or FPGA development boards. Then the hardware description is transferred to the standard-cell IC. Since this approach typically permits only a functional but not a real-time verification of the circuit, it has an inherent risk in that the performance level is conclusively established only with the final standard-cell IC.

ISSP offers a novel concept for clock wiring. The clocks are prewired and very

well balanced, so that system frequencies up to 300MHz (globally) and up to 400MHz (locally) can be obtained. Up to 2 global and 8 local clocks can be connected to this clock system. ISSP is thus eminently suited for designing high-performance ASICs.

Design for testability

Another important issue is design for testability (DFT). This means the implementation of comprehensive test methods from the very beginning of circuit development. ISSP achieves testability close to 100% by means of a preimplemented scan technology. In addition, it provides built-in self test (BIST) methodologies for existing prediffused SRAMs and a boundary scan logic for input and output signals. An ISSP-based circuit design thus produces a fully tested ASIC, with all the actual work done by NEC. The entire test logic is integrated and prediffused on the ISSP master.

ISSP inevitably results in a greater chip area being used than for a standard-cell IC, owing to the fact that not all CMGs are always used completely. On the other hand, because ISSP was developed on the basis of CB-12 standard-cell ASIC technology, it is relatively simple to transfer the design to standard-cell IC technology, as soon as order volumes grow and an absolutely area-optimized design is required.

Initially ISSP is available in three different sizes in a tape-automated bonding ball grid array (TBGA) packages. The portfolio will be expanded in the near future to include quad flat package (QFP) and other BGA packages, such as flipchip BGAs.

With ISSP, NEC is attempting to give customers the option of using high-performance ASICs in applications that used to be excluded for cost reasons, because the volumes were too small to recoup the high development costs.

ISSP will make you change your habits.

The new ASIC platform ISSP:

0.13 μm performance – for lowest cost and shortest time to market



Master	Usable Logic	Embedded SRAM Blocks (16 Kbit)	APLLs		DLLs
			High Speed	Middle Speed	
PD65701	-200K	16	3	1	8
PD65702	-500K	48	3	1	8
PD65703	-1,100K	64	3	1	16

Test something better for a change. ASIC performance at a tenth of the usual costs. ASIC time to market slashed by a massive 75%. A new ASIC platform concept for a development environment as efficient as it is user-friendly. In short: ISSP from NEC. With this Instant Silicon Solution Platform we've reinvented ASICs. If that's not a reason to change your habits, what is?

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