

TENSILICA DIAMOND CPU CONTROLLER CORES FOR NEC ELECTRONICS GATE ARRAYS

Tensilica® Diamond Standard processor cores are available directly from NEC Electronics America for its CMOS-12M, CMOS-10HD, CMOS-9HD and EA-9HD series gate arrays. By making the cores and gate arrays available under one development and licensing agreement, NEC Electronics America can streamline the design and licensing process and offer ASIC designers a more complete solution—with NRE costs that are substantially lower than NRE costs for cores used in cell-based designs.

The four Diamond Standard cores available with NEC Electronics gate arrays, the 106Micro, 108Mini, 212GP and 232L, are ready-to-use synthesizable cores. These area-efficient, low-power processors are based on Tensilica's highly efficient Xtensa configurable and extensible processor architecture, proven in hundreds of SoC designs. NEC Electronics gate arrays designed with Tensilica's cores are ideal for applications ranging from low-power handsets to high-performance communication equipment.

NEC Electronics gate arrays along with the Diamond Standard cores provide a versatile and high-performance computing architecture for custom-logic design, a combination that enables designers to customize and differentiate their products quickly, efficiently and cost effectively.



106Micro RISC CPU CONTROLLER CORE

Features

- › Smallest, lowest-power 32-bit RISC controller core
- › Cache-less design with memory protection unit
- › 5-stage pipeline
- › 24-/16-bit ISA with modeless switching
- › Iterative 32×32 multiplier
- › Separate instruction and data memory interfaces
- › Integrated interrupt controller with 15 interrupts at two priority levels
- › Integrated timer
- › On-chip debugging hardware
- › Embedded trace support
- › AHB-lite and AXI bridges
- › Comparable to ARM7TDMI-S™ CPU and, except for DSP functionality, to ARM966E-S™ and ARM968E-S™ CPUs

Benefits

- › Easy migration from 8- and 16-bit microcontrollers
- › Lower total system costs due to smaller size, higher performance, and better code density
- › Deterministic real-time operation through optional single-cycle local instruction and data SRAM blocks
- › Multiplier provides arithmetic and DSP performance
- › Drop into existing AMBA™ systems

The Tensilica Diamond 106Micro CPU controller core is designed for small die areas in extremely low-power applications and is available directly from NEC Electronics America for CMOS-12M, CMOS-10HD, CMOS-9HD and EA-9HD gate arrays. This cache-less controller is ideal for designers looking for a basic 32-bit controller, particularly for those migrating from an 8- or 16-bit controller. The core enables SoC architects to integrate an efficient CPU in their designs, and provides the added benefit of extremely fast time to market.

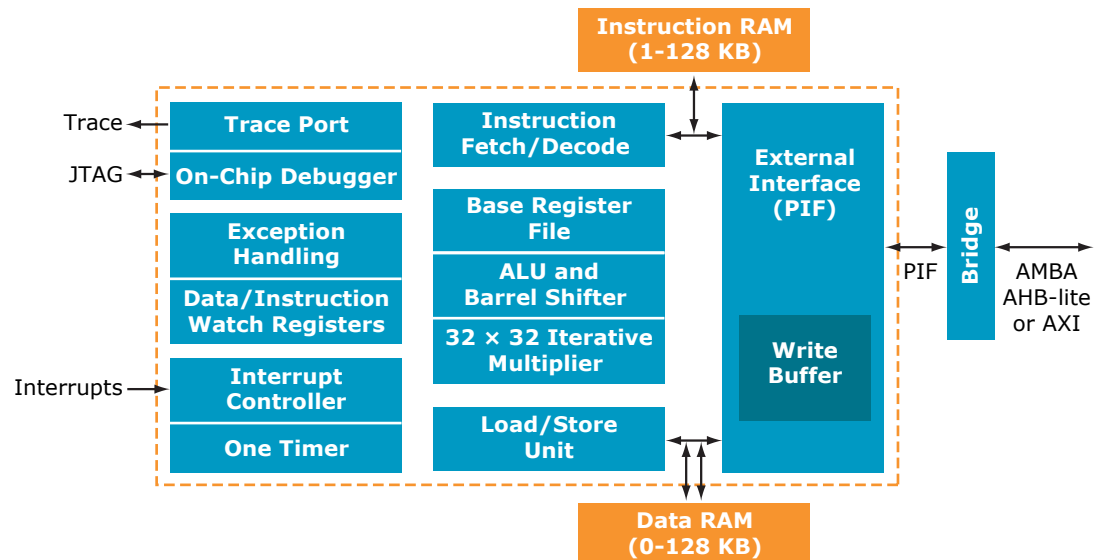
Projected Performance of the Diamond 106Mini core in NEC Electronics gate array series

Gate Array Series	VDD (V)	Frequency* (MHz)	Size (Gates)	Dhrystone MIPS/MHz	Instruction Width (Bits)
CMOS-12M	1.5	200	32K	1.2	16/24
CMOS-10HD	2.5	90			
	1.8	50			
CMOS-9HD/EA-9HD	3.3	60			

* Frequency is based on projected data.

Although the Diamond 106Micro is extremely small, it employs a 5-stage pipeline so it can achieve 200 MHz* in CMOS-12M gate arrays. By modelessly switching between 24- and 16-bit narrow instructions, it achieves a much higher code density than other 32-/16-bit architectures.

The local, tightly coupled instruction and data memory on the Diamond 106Micro can be used to store performance-sensitive code and data, for example, to achieve high performance in interrupt handlers. The Diamond 106Micro has an iterative, multi-cycle (non-pipelined) 32×32 multiplier that greatly enhances performance on arithmetic and DSP code. A non-windowed 16-entry AR register file keeps area low. The Diamond 106Micro has an integrated timer and an integrated interrupt controller with 15 interrupts that simplify system design since no external hardware need be added for these functions.



108MINI RISC CPU CONTROLLER CORE

Features

- › Small-size, ultra-low-power RISC controller
- › Cacheless design with memory protection unit
- › 32-bit integer divider
- › Single-cycle instruction interface and dual-data local SRAM interface
- › Nonmaskable interrupt
- › Three timers
- › Fully synthesizable; portable to any process technology
- › On-chip debugging hardware
- › Programmable I/O ports
- › Comparable to ARM7TDMI-S™ CPU and, except for DSP functionality, to ARM966E-S™ and ARM968E-S™ CPUs

Benefits

- › Lower total system costs due to smaller size, higher performance, and better code density than competitive products
- › Rich interrupt architecture that reduces the need for an external interrupt controller
- › Programmable ports that reduce external control logic and speed up I/O transfers
- › FPGA system prototyping support that reduces design risk
- › Deterministic real-time operation through optional single-cycle local instruction and/or data SRAM

The Tensilica fully synthesizable 32-bit Diamond 108Mini RISC CPU controller core is available directly from NEC Electronics America for its CMOS-12M, CMOS-10HD, CMOS-9HD, and EA-9HD series gate arrays. The Diamond 108Mini features class-leading low power consumption for portable applications.

Projected Performance of the Diamond 108Mini core in NEC Electronics gate array series

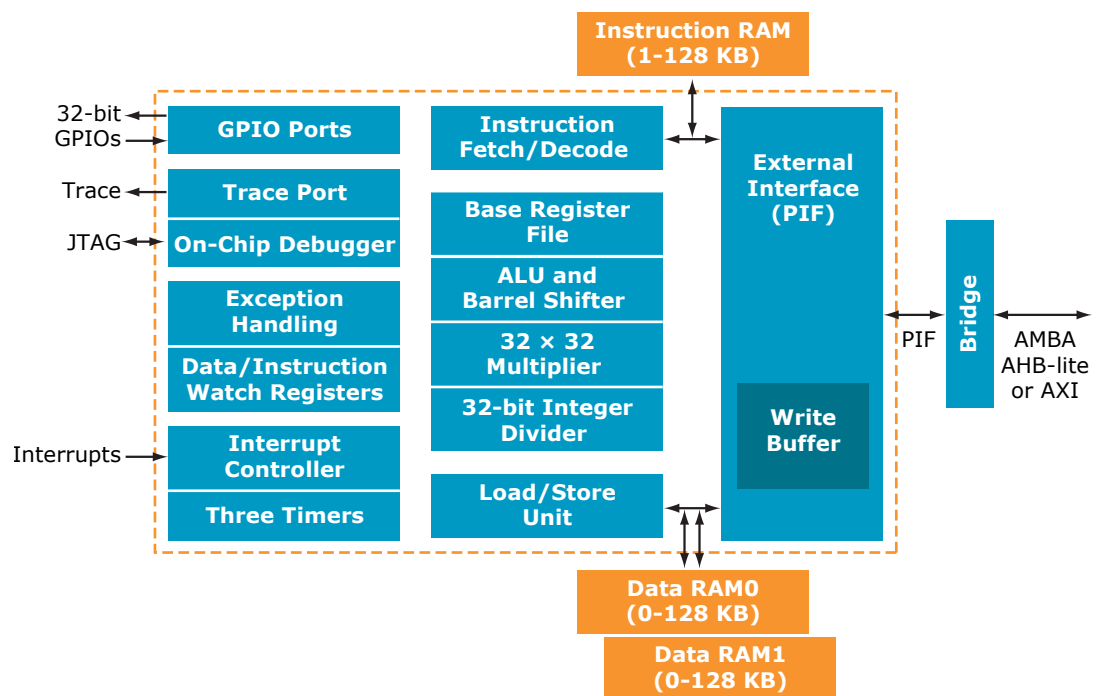
Gate Array Series	V _{DD} (V)	Frequency* (MHz)	Size (Gates)	Dhrystone MIPs/MHz	Instruction Width (Bits)
CMOS-12M	1.5	200	50K	1.2	16/24
CMOS-10HD	2.5	90			
	1.8	50			
CMOS-9HD/ EA-9HD	3.3	60			

* Frequency is based on projected data.

In CMOS-12M gate arrays, the 108Mini offers extremely high performance at 200 MHz*, and is capable of handling control-plane applications where minimal die area is the most important system design parameter, although advanced debugging features are supported.

The Diamond 108Mini also improves upon interrupt latency and has deterministic behavior in applications with hard real-time constraints. Thirty-two base registers are windowed 16 at a time, which enables much faster context switching due to reduced stack operations. Local single-cycle SRAM allows time-critical code to be placed near the CPU. Dual local data SRAM interfaces enable processor access to one bank of RAM while an external direct memory access (DMA) operation can operate on the other bank.

The Diamond 108Mini is one of the smallest, lowest-power-consuming 32-bit RISC controllers on the market. Despite its small size, it achieves performance levels comparable to those of much larger, much more complex CPUs.



212GP RISC CPU CONTROLLER CORE

Features

- › Small-size, high-performance, low-power-consuming CPU core
- › Five-stage pipeline
- › Single-cycle 16 × 16-bit MAC
- › DSP instructions
- › 32-bit integer divider
- › 8 KB, 2-way set associative instruction and data caches; programmable write-through or write-back transfers
- › Local single-cycle instruction and data SRAM interfaces
- › Non-maskable interrupt
- › Three timers
- › High-speed peripheral port
- › Comparable to ARM946E-S™ CPU

Benefits

- › Flexible memory architecture adaptable to an extremely wide range of applications
- › On-chip debugger that decreases time to market
- › DSP functions that lower system costs (by eliminating the need for a DSP core)
- › Higher performance and smaller die size than competitor products—lower system costs

The high-performance, versatile, fully synthesizable 32-bit Tensilica Diamond 212GP RISC CPU controller core is available directly from NEC Electronics America for its CMOS-12M, CMOS-10HD, CMOS-9HD and EA-9HD series gate arrays. In addition to efficient in terms of area and power, the Diamond 212GP's local memory architecture provides outstanding flexibility and performance. Users can take advantage of Tensilica's lockable cache and attach a single-cycle instruction or data SRAM of any size—up to 128 KB.

Projected Performance of the Diamond 212GP core in NEC Electronics gate array series

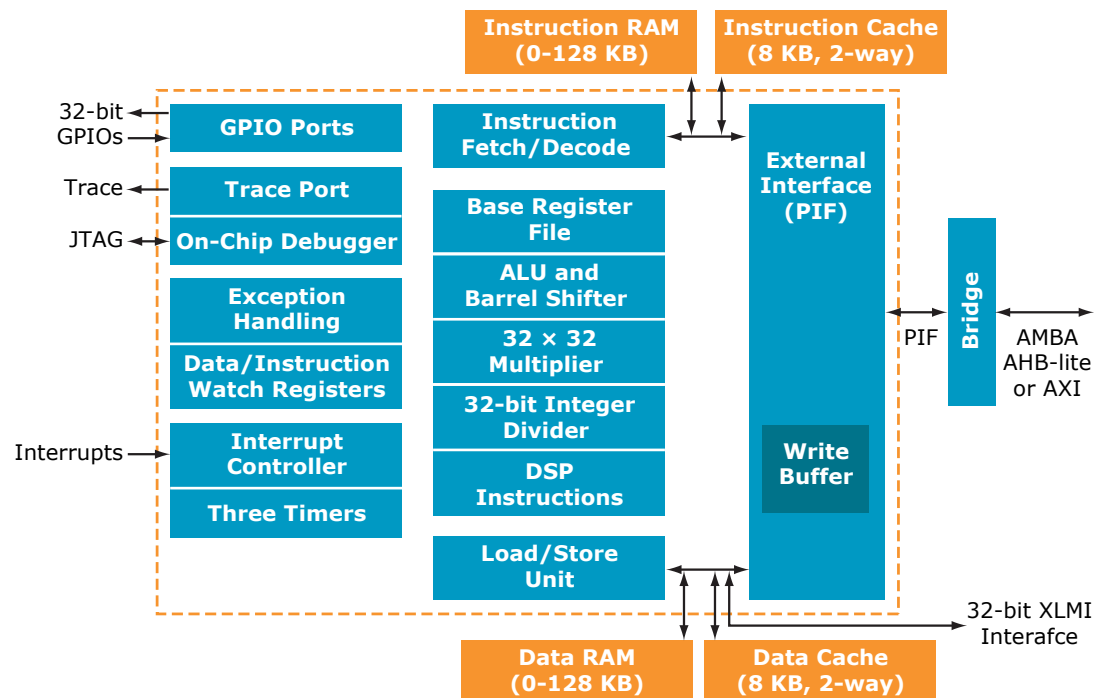
Gate Array Series	VDD (V)	Frequency* (MHz)	Size (Gates)	Dhrystone MIPs/MHz	Instruction Width (Bits)
CMOS-12M	1.5	180	80K	1.3	16/24
CMOS-10HD	2.5	80			
	1.8	45			
CMOS-9HD/EA-9HD	3.3	50			

* Frequency is based on projected data.

Since 212GP target applications are controller related, interrupt options are extremely important. The 212GP core includes a nonmaskable interrupt for critical system events and five levels of external, software, and timer interrupts that ease the development of software interrupt handlers and the design of hardware-based external interrupt handlers.

In addition, on-chip DSP hardware support, consisting of a single-cycle 16-bit × 16-bit MAC unit, four dedicated 32-bit registers and a 40-bit accumulator, eliminates the need to include a separate DSP in the system design. Additionally, there is support for zero-overhead looping, clamps (saturating arithmetic), maximum/minimum value, normalize, and sign extend operations.

The Diamond 212GP provides an ideal combination of performance, area, and code efficiency for controller applications requiring mid to high performance.



232L RISC CPU CONTROLLER CORE

Features

- › Smallest, lowest-power Linux-ready CPU in its class
- › Linux-compatible memory management unit
- › Five-stage pipeline
- › Single-cycle 16 × 16-bit MAC
- › DSP instructions
- › 32-bit integer divider
- › 16 KB, 4-way set-associative instruction and data caches; programmable write-through or write-back transfers
- › Nonmaskable interrupt
- › Three timers
- › Comparable to ARM926EJ-S™ CPU without Java support.

Benefits

- › On-chip debug decreases time to market
- › DSP functions supported in processor, lowers system costs (eliminate a DSP core)
- › Higher performance and smaller die size than other applications processors, lowers system costs

The Tensilica Diamond 232L CPU controller core is available directly from NEC Electronics America for its CMOS-12M, CMOS-10HD, CMOS-9HD and EA-9HD series gate arrays.

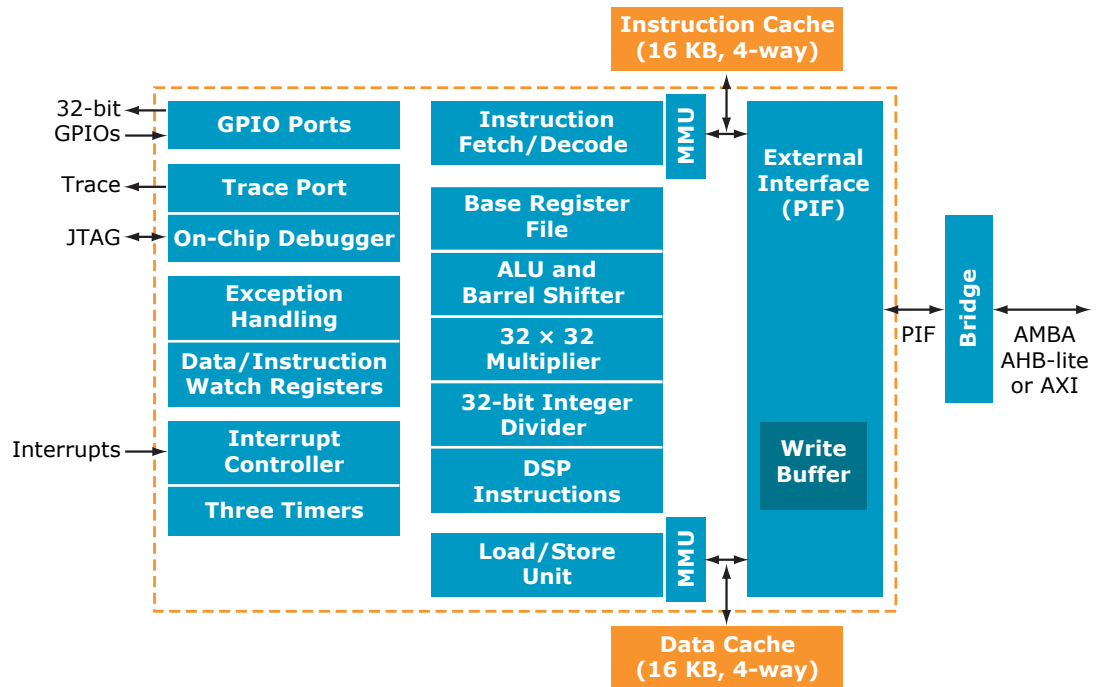
Similar to the Diamond 212GP core, the 232L additionally has a full-featured memory management unit (MMU) and is targeted to application processing using operating systems such as embedded Linux with 4-way set-associative 16 KB instruction and data caches.

Projected Performance of the Diamond 232L core in NEC Electronics gate array series

Gate Array Series	V _{DD} (V)	Frequency* (MHz)	Size (Gates)	Dhrystone MIPS/MHz	Instruction Width (Bits)
CMOS-12M	1.5	180	90K	1.3	16/24
CMOS-10HD	2.5	80			
	1.8	45			
CMOS-9HD/ EA-9HD	3.3	50			

* Frequency is based on projected data.

The MMU provides instruction and data translation lookaside buffers (TLBs), which manage virtual-to-physical address mapping. In addition to address translation, the MMU provides four different privilege levels (for memory protection), variable page sizes and multiple access modes. Combining the MMU with a flexible interrupt architecture and high performance, the Diamond 232L can easily meet the needs of a complex system running numerous applications.



DIAMOND CORE ARCHITECTURE AND SUPPORT

Instruction Set Architecture

The Tensilica Diamond Standard Series CPU cores incorporate the Xtensa instruction set architecture (ISA), a 32-bit ISA optimized for embedded designs. In addition to a 32-bit arithmetic logic unit (ALU), 32 general-purpose physical registers, six special-purpose registers, and 80 base instructions, Diamond Standard CPUs also feature compact 16- and 24-bit (rather than 32-bit) RISC instruction encoding. Depending on the actual code, Diamond Standard Series CPU cores enable designers to achieve 10% to 40% smaller code size compared to conventional RISC cores, resulting in higher performance, smaller memory sizes, and better power dissipation—key parameters in cost-sensitive, highly integrated SOC designs.

The Xtensa ISA's 16- and 24-bit encoding also provides powerful branch instructions and bit manipulations that include funnel shifts and field-extract operations. Tensilica's XCC C/C++ compiler generates an optimized combination of 24-bit and 16-bit instruction encoding in a single instruction stream. There is no CPU mode switching between 16- or 24-bit instruction types. Firmware developers need not decide which parts of their code should be compiled with instruction encodings of different lengths.

Comprehensive Software Tool Support

Tensilica offers a comprehensive tool kit that will speed the development process for software developers. Tensilica's Eclipse-based Xtensa Xplorer™ graphical user interface (GUI) serves as the cockpit for the entire development experience, integrates the compiler tool chain as well as the instruction set simulator (ISS), and interfaces to hardware emulation/development boards.

Tensilica's XCC C/C++ compiler is based on the GNU compiler front end with a highly customized code generation back end targeting Tensilica's instruction set. XCC employs sophisticated multilevel optimizations to increase code execution speed and reduce code size.

Also included in the Xplorer environment are a software project manager, code profiling tools, a source code editor, a debugger, a performance-modeling tool, and the optional XTMP (Xtensa Modeling Protocol) for simulation of multiple processor SOCs. For more information please visit www.tensilica.com.



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NEC Electronics design centers are strategically located around the United States in Boston, Chicago, Dallas, Portland and Santa Clara.

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Printed in U.S.A. on recycled paper using soy ink.

Document No. A18755EU2V0PF00