NEC Electronics America

Using Custom Silicon to Develop Lower-Power, Lower-Cost, and More Secure Products for the Industrial Market

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Today's industrial market is composed of many diverse applications. In fact, electronic systems are integrated into equipment destined for such widely differing segments as building and factory automation, medical electronics, power, security and transportation, to name a few. This diversity poses an interesting challenge for the electronics supplier, as each segment has a unique environmental framework that influences the electronic device's features and performance. Despite these differences, there is common ground in terms of the design requirements facing engineers working in the industrial market today. Regardless of the end application, engineers must contend with the demand for products with longer life spans, higher reliability and lower costs and be able to easily design and develop product variations.

Conventional means of addressing these requirements have relied on the use of FPGAs, because they are convenient for prototyping and production of a product. Unfortunately, FPGAs alone do not provide the optimal solution industrial designers demand. What's required is a new approach that employs the use of a gate array ASIC in combination with an FPGA. This combination can drastically reduce overall component costs by up to 80 percent and offers a multitude of other benefits such as lower power and increased security.

Understanding the Trends

No other semiconductor market is as diverse as the industrial market, and yet it is exactly this diversity that dictates the need for electronic devices to adhere to high standards for quality, operate over wide temperature ranges and, depending on the application, to feature low standby and dynamic power. Perhaps even more importantly, today's industrial market requires:

- **Products with longer life spans**
  In the industrial market, electronic products are required to support a long service life (of 7, 10 or 15 years for standard products versus less than two years for some consumer products).

- **Methods for easily developing design and product variations**
  To support the diversity of the industrial market and remain competitive, engineers must be able to accommodate a wide range of customer requirements. As a result, they require a method for easily creating design and product variations.
- **High reliability**
  Electronic products used in the industrial market must operate for a long period of time and accommodate long maintenance cycles, making high reliability critical.
- **Low cost**
  As with any market these days, minimizing the cost of electronic products is always a crucial factor. In the industrial market, engineers demand not only low overall system costs, but low NRE costs as well.

Traditionally, FPGAs have been the device of choice to address these requirements. After all, they offer a number of benefits in terms of performance, reliability and long-term maintenance, which make them well-suited for the industrial market. Also, an FPGA is a relatively low-cost option, since only one device is needed to start a design. In addition, the flexibility and rapid prototyping capabilities of FPGAs enable engineers to hit the ground running and therefore enable fast time to market.

Despite these benefits, the disadvantages associated with FPGAs mean that they are not always the best solution for today's industrial market. By their very nature, they burn a lot of power and are prone to piracy—an especially problematic issue given that system boards are now shipping into many regions around the world and can be easily copied. FPGAs also do not address the need for longer life spans and their programmable interconnects require a substantial amount of die area. In fact, when compared to other semiconductor solutions, FPGAs tend to be noisy (emitting greater electromagnetic interference), run slower and have higher overall system costs.

Another option—the gate array ASIC—has also had its share of drawbacks, being viewed by some as a less than optimal approach to ASIC design, primarily due to its somewhat lower density and performance than semiconductor solutions. These days however, those shortcomings are no longer valid (Table 1). Today's gate arrays offer a host of benefits that make them especially advantageous to the industrial engineer, including high performance, high gate density, low power, low piece price, low NRE costs, fast turnaround times and piracy protection. Given the fast-paced dynamic of today's industrial market, using a device such as a gate array ASIC has become key to gaining a competitive edge.

Specification	Gate Array vs. FPGA
Logic performance	Often three to five times higher than FPGA logic; more than 200 MHz at 15 levels of logic with routing
Small footprint	Smaller package for a given gate count starting at 5 × 5 mm Low profile of 0.69 mm and up High logic density that can consolidate multiple chips No configuration memory required
Logic density	As high as 20M "system gates" or 2M ASIC gates
Operating power	As much as 10× lower than FPGAs
Standby power	As much as 20–1000× lower than FPGAs
Radiated electromagnetic interference (EMI)	Inherently lower due to the low power consumed Slew rate-controlled buffers that quiet down clock edges Available spread-spectrum clock generator (SSCG) that reduces spikes further Available embedded capacitors that reduce power supply noise
Reconfiguration time	Effectively zero; can cost-effectively store multiple configurations, switching over in one clock
Soft error rate (SER) / Single-event upsets (SEUs)	Can be more than two orders of magnitude lower (most families are less than 0.2 FIT per kilobit of memory); eliminates configuration memory, the source of most soft errors
Hardware failure rate	Typically two to ten times lower; as low as 3 FITS per device

Table 1. While some FPGA designs are smaller than ASIC designs, many of today's FPGA designers can be characterized as risk takers who are pushing the design envelope. Today, thanks to their myriad benefits, gate arrays now offer a good solution with compelling value—even when compared to FPGAs.

A Better Alternative

Today's industrial requirements call for a solution that is more powerful than either the FPGA or gate array ASIC alone can deliver. They require a solution that effectively couples an FPGA with a gate array ASIC, which can be accomplished in one of two ways. For any given design, an engineer can divide the system board into two sections—one for the FPGA and the other for the gate array ASIC. Alternatively, FPGAs and gate array ASICs can co-exist within a company's product portfolio.

In both cases, FPGAs would occupy the variable portion of the system board, and bring all of the development advantages associated with their flexibility. The gate array ASIC, on the other hand, would reside where it is the most cost- and performance-effective, and provide all of its advantages, such as quality, security, density, high performance, low development and NRE costs, and unit costs starting as low as $1. Even at this price point, gate arrays offer a significant advantage in density. A similarly priced CPLD holds only five percent as much logic.

The gate array would also enable a fast turnaround time with engineering samples available in as little as one week. More importantly, the combination of the FPGA and gate array ASIC effectively addresses the industrial market's four critical requirements for longer life spans, easy product variation or differentiation, high reliability and low cost.

DESIGN EXAMPLES

The combined FPGA and gate array ASIC solution can be used in a range of applications to address specific needs in the industrial market. Specific design examples include:

- **Replacement for end-of-life (EOL) components**
  Successful industrial product designs often remain in the marketplace for a long period of time. Yet, replacing components that have reached their EOL can be problematic. Because of their staying power, gate array ASICs can be an ideal solution to EOL components. Pin-compatible replacements based on gate arrays are also available, eliminating the need to respin an existing system board and adding many years to a product's life cycle (Figure 1).

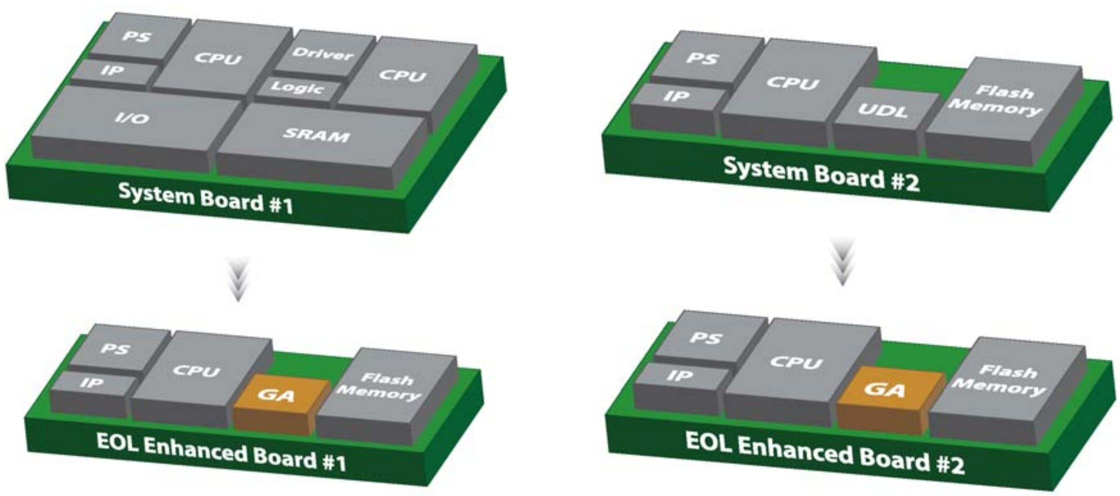

Figure 1. When replacing EOL components, finding products that support legacy operating voltages can be an issue. In such cases, NEC Electronics' CMOS-N5 gate arrays offer a key advantage: 5V-only operation for both core logic and I/Os, as shown in the EOL Enhanced Board #1. While the integration of this functionality into a single chip can present some risks, NEC Electronics also provides pin-compatible replacements based on gate arrays for the 8251 UART and 8254 programmable timer unit as demonstrated in EOL Enhanced Board #2 above.

- **Consolidation of several devices into one**

  Combining multiple FPGAs and other devices into a single gate array provides a number of benefits (Figure 2). To begin with, the engineer realizes the lower price and lower power consumption associated with gate arrays. Eliminating the buffers and circuits duplicated in multiple devices achieves further savings for both price and power. In addition, using a single gate array allows engineers to reduce board size.

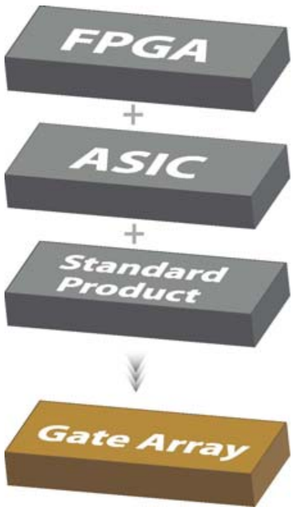

Figure 2. Consolidating multiple FPGAs and other devices into a single gate array reduces board size, cost and power.

- **Protecting products from piracy**

  ROM cartridges and devices with embedded memory—including the stored bit streams used for programming FPGAs—can be read and duplicated easily. Unfortunately, piracy has become all the more prevalent due to an increasing number of system boards being shipped around the world. The gate array works to prevent this piracy by acting as a security key in which the stored software works only if the gate array is present (Figure 3). As an added benefit, the gate array itself is exceedingly difficult, if not impossible, to reverse engineer.

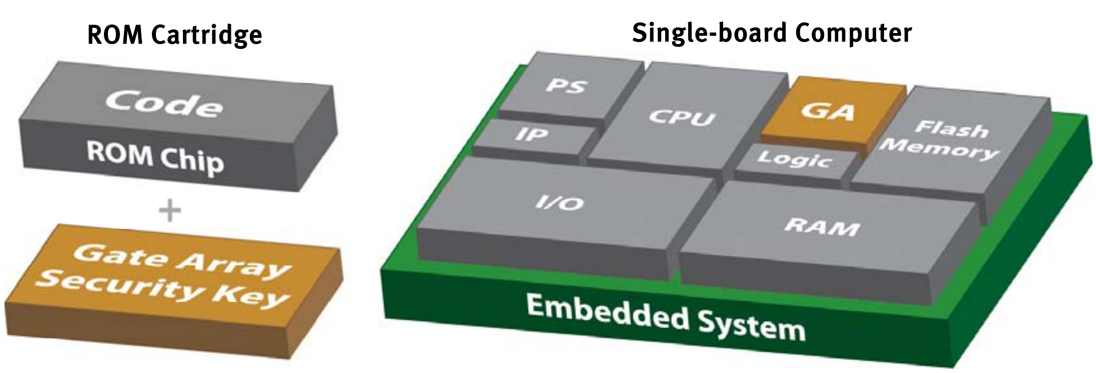

Figure 3. The security 'key" in this graphic refers to the gate array. It must be present for the system software to work.

Conclusion

Today's diverse industrial market presents engineers with a number of challenging requirements for higher reliability, lower costs and longer life spans. While designers have traditionally addressed many of these requirements with an FPGA-only solution, a new approach that combines an FPGA with a gate array ASIC offers a slew of benefits. Using this approach, engineers can realize up to 80 percent lower component costs, smaller footprints and faster turnaround times. Additionally, this solution enables low power (both dynamic and static), increased security and high reliability. Such capabilities make the FPGA and gate array ASIC solution the most optimal answer to meeting the needs of today's industrial market.